POWER SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2006-297369, filed on Nov. 1, 2006; the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to a power semiconductor device, and more particularly to a power semiconductor device having a superjunction structure.

[0004] 2. Background Art

[0005] The ON resistance of a power semiconductor device such as a vertical power MOSFET (metal oxide semiconductor field effect transistor) greatly depends on the electric resistance of its conduction layer (drift layer). The dopant concentration that determines the electric resistance of the drift layer cannot exceed a maximum limit, which depends on the breakdown voltage required for a pn junction between the base layer and the drift layer. Thus there is a tradeoff between the device breakdown voltage and the ON resistance. Improving this tradeoff is important for improving the performance of low power consumption devices. This tradeoff has a limit determined by the device material. Overcoming this limit is the way to realizing devices with low ON resistance beyond existing power devices.

[0006] As an example MOSFET overcoming this limit, a MOSFET having a structure called a superjunction structure is known, where p-pillar layers and n-pillar layers are alternately buried in the drift layer (see, e.g., JP-A 2004-282007 (Kokai)). In the superjunction structure, a non-doped layer is artificially produced by equalizing the amount of charge (amount of impurities) contained in the p-pillar layer with the amount of charge contained in the n-pillar layer. Thus, while holding high breakdown voltage, current is passed through the highly doped n-pillar layer. Hence low ON resistance beyond the material limit can be achieved.

[0007] Thus, in a vertical power MOSFET, the superjunction structure can be used to realize an ON resistance/breakdown voltage tradeoff beyond the material limit. By such an improved tradeoff, the chip area can be decreased with the ON resistance kept at a prescribed value. In this case, the chip area is decreased with the operating current kept constant, which results in increasing the density of current flowing in the chip. Hence the decrease in chip area also results in increasing current density during bipolar operation of the vertical power MOSFET, such as during avalanche breakdown and during recovery operation of the built-in diode. If the current density during bipolar operation increases, the carrier density in the device also increases. If the carrier density in the device increases by a certain degree or more, carrier charging results in increasing electric field strength and causing current concentration, and the device leads to breakdown. That is, another problem has arisen where the decrease of ON resistance and the reduction of chip area due to the superjunction structure lead to the increase of current density, causing the decrease of avalanche withstand capability and recovery withstand capability.

SUMMARY OF THE INVENTION

[0008] According to an aspect of the invention, there is provided a power semiconductor device including: a semiconductor substrate; a gate insulating film; a control electrode insulated from the semiconductor substrate by the gate insulating film; a first main electrode provided on a lower surface side of the semiconductor substrate; and a second main electrode provided on an upper surface side of the semiconductor substrate, the semiconductor substrate including: a first first-conductivity-type semiconductor layer with its lower surface connected to the first main electrode; a second first-conductivity-type semiconductor layer and a third second-conductivity-type semiconductor layer formed on the first first-conductivity-type semiconductor layer and alternately arranged parallel to the upper surface of the semiconductor substrate; a trench formed in a directly overlying region of the third second-conductivity-type semiconductor layer, with part of the second main electrode buried in the trench; a fourth second-conductivity-type semiconductor layer selectively formed in a surface of the second first-conductivity-type semiconductor layer and connected to the second main electrode; a fifth first-conductivity-type semiconductor layer selectively formed in a surface of the fourth second-conductivity-type semiconductor layer and connected to the second main electrode; and a sixth second-conductivity-type semiconductor layer formed at a bottom of the trench and connected to the second main electrode, impurity concentration in the sixth second-conductivity-type semiconductor layer being higher than impurity concentration in the fourth second-conductivity-type semiconductor layer, and lower surface of the sixth second-conductivity-type semiconductor layer being located below lower surface of the fourth second-conductivity-type semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a cross-sectional view schematically illustrating a power MOSFET according to a first embodiment of the invention;

[0010] FIG. **2** is a cross-sectional view schematically illustrating a power MOSFET according to a first variation of the first embodiment;

[0011] FIG. **3** is a cross-sectional view schematically illustrating a power MOSFET according to a second variation of the first embodiment;

[0012] FIG. **4** is a cross-sectional view schematically illustrating the configuration of a power MOSFET according to a second embodiment of the invention, and schematic graphs illustrating impurity concentration (pillar concentration) in its n-pillar layer and p-pillar layer and electric field therein in correlation with position along the thickness direction;

[0013] FIG. **5** is a cross-sectional view schematically illustrating the configuration of a power MOSFET according to a variation of the second embodiment, and schematic graphs illustrating impurity concentration (pillar concentration) in its n-pillar layer and p-pillar layer and electric field therein in correlation with position along the depth direction;

[0014] FIG. **6** is a cross-sectional view schematically illustrating the configuration of a power MOSFET according to a third embodiment of the invention;